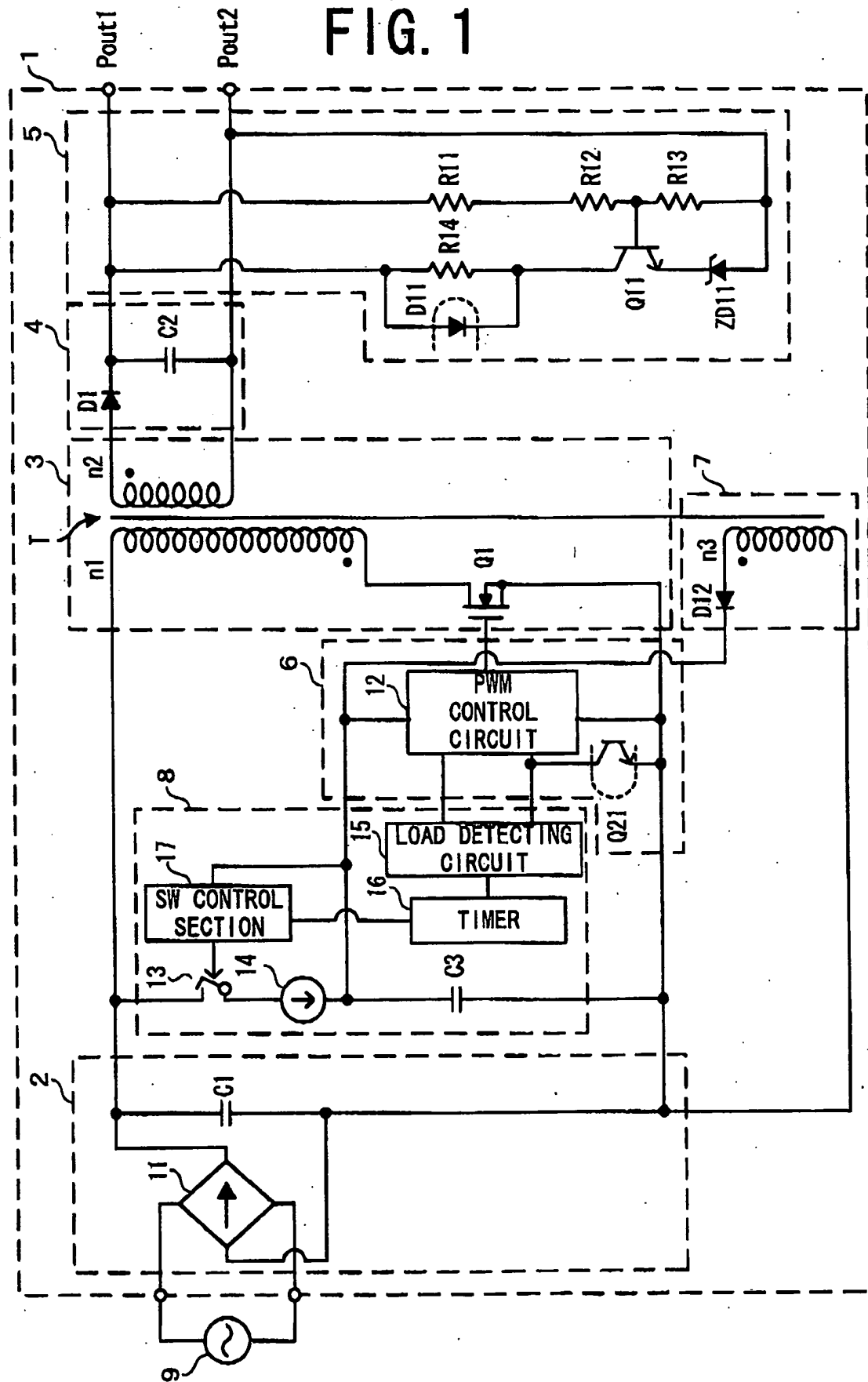
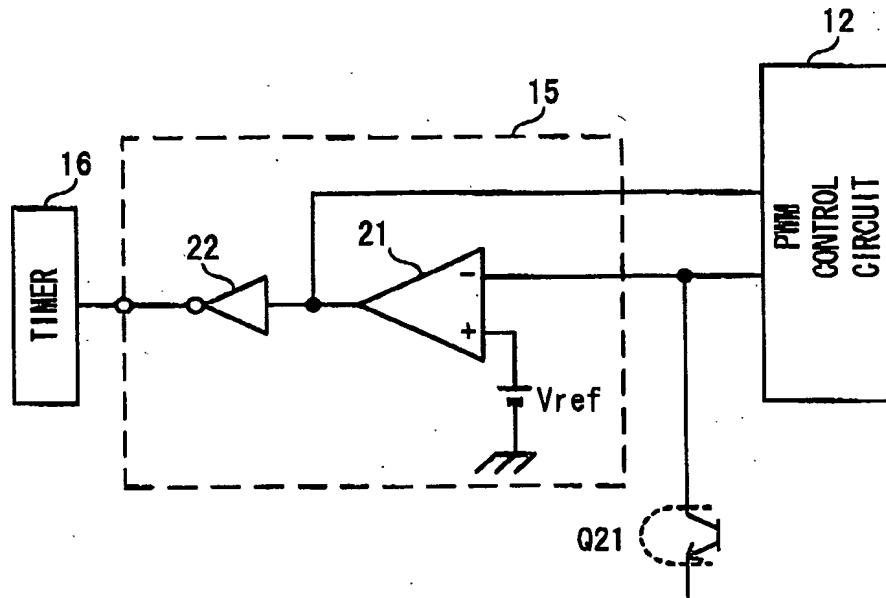


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FIG. 1



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FIG. 2

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FIG. 3

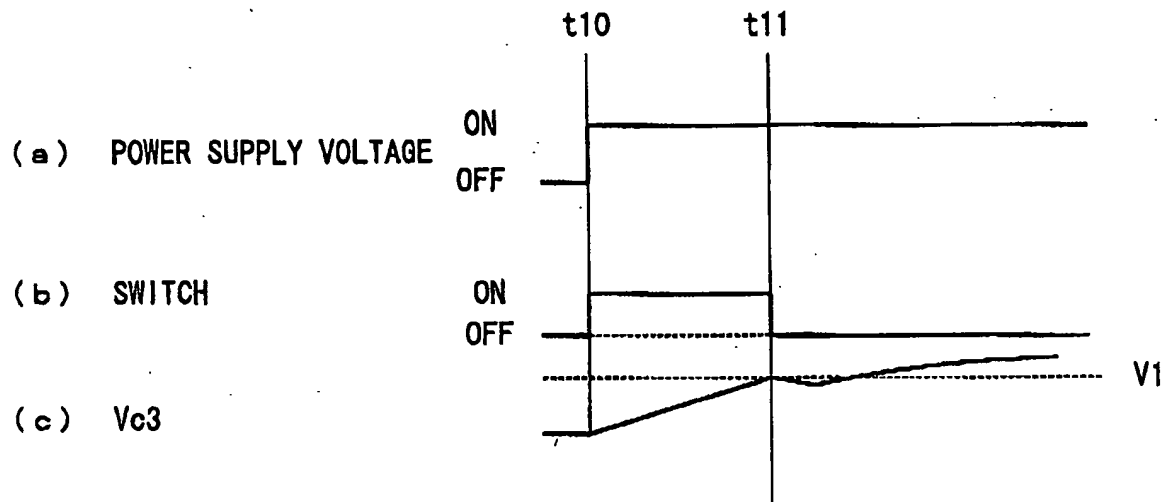
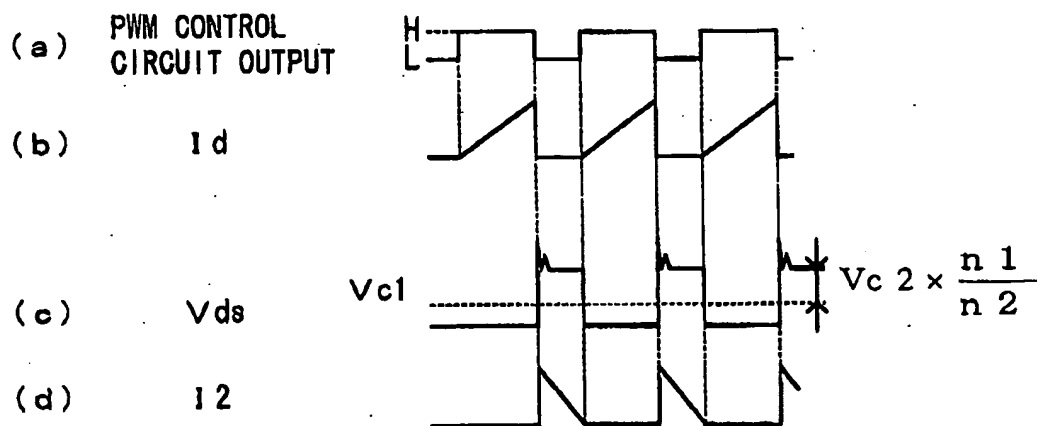


FIG. 4

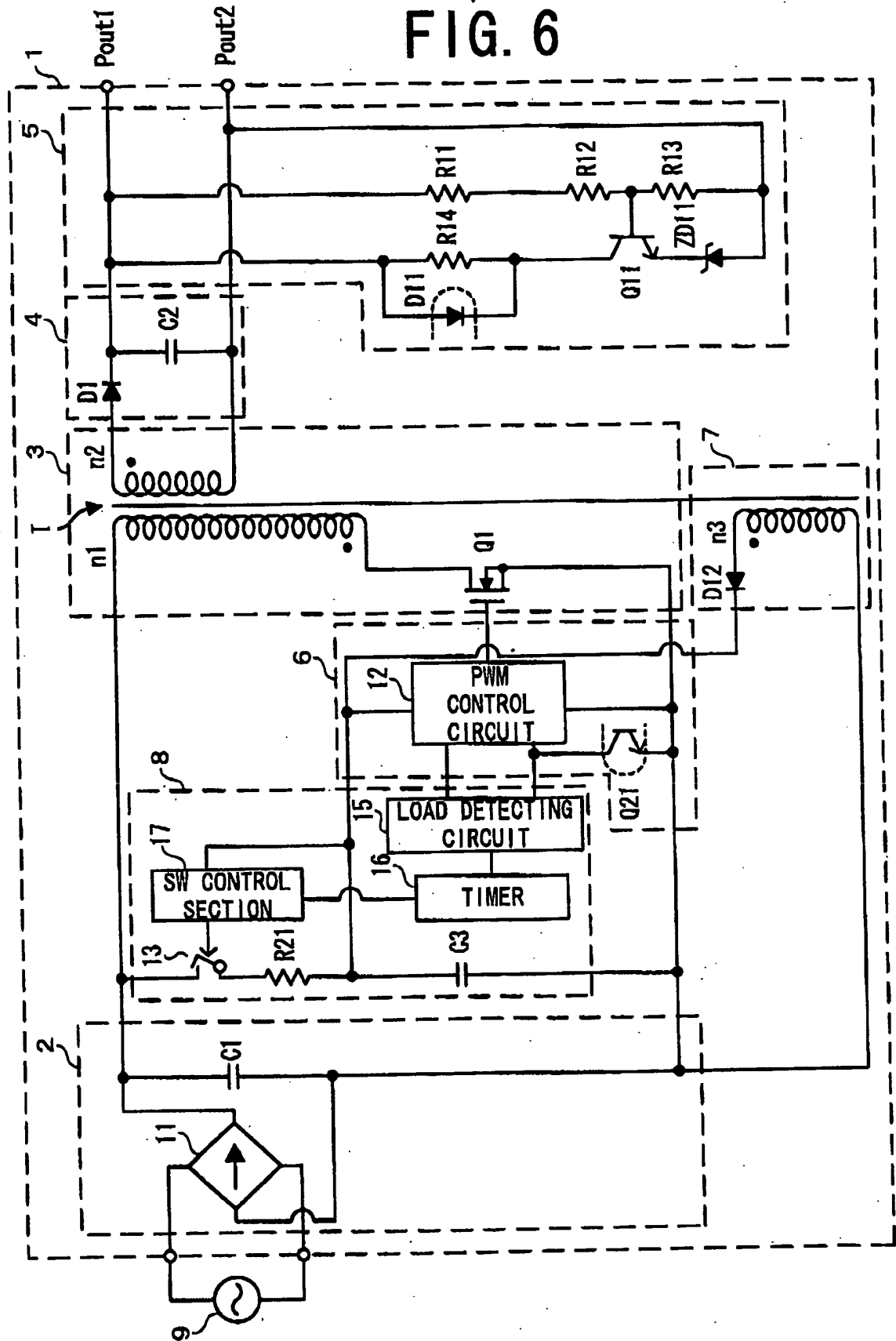


The timing diagram illustrates the operation of the load detecting circuit across three time intervals:  $t_{21}$  to  $t_{22}$  (Heavy Load),  $t_{22}$  to  $t_{23}$  (Light Load), and  $t_{23}$  to  $t_{24}$  (Heavy Load). The waveforms are as follows:

- (a) SWITCH:** A square wave that is ON from  $t_{21}$  to  $t_{22}$ , OFF from  $t_{22}$  to  $t_{23}$ , and ON from  $t_{23}$  to  $t_{24}$ .
- (b)  $V_{c3}$ :** A voltage waveform that rises sharply at  $t_{21}$ , remains high until  $t_{22}$ , falls sharply at  $t_{22}$ , remains low until  $t_{23}$ , rises sharply at  $t_{23}$ , and remains high until  $t_{24}$ .
- (c)  $V_{out}$ :** A voltage waveform that is high from  $t_{21}$  to  $t_{22}$ , drops to a lower level at  $t_{22}$ , and returns to the high level at  $t_{23}$ .
- (d)  $I_{out}$ :** A current waveform that is high from  $t_{21}$  to  $t_{22}$ , drops to a lower level at  $t_{22}$ , and returns to the high level at  $t_{23}$ .
- (e)  $V_{pc}$ :** A voltage waveform that is high from  $t_{21}$  to  $t_{22}$ , drops to a lower level at  $t_{22}$ , and returns to the high level at  $t_{23}$ .
- (f) LOAD DETECTING CIRCUIT OUTPUT:** A digital output that is high from  $t_{21}$  to  $t_{22}$ , low from  $t_{22}$  to  $t_{23}$ , and high from  $t_{23}$  to  $t_{24}$ .
- (g) TIMER OUTPUT:** A digital output that is high from  $t_{21}$  to  $t_{22}$ , low from  $t_{22}$  to  $t_{23}$ , and high from  $t_{23}$  to  $t_{24}$ .

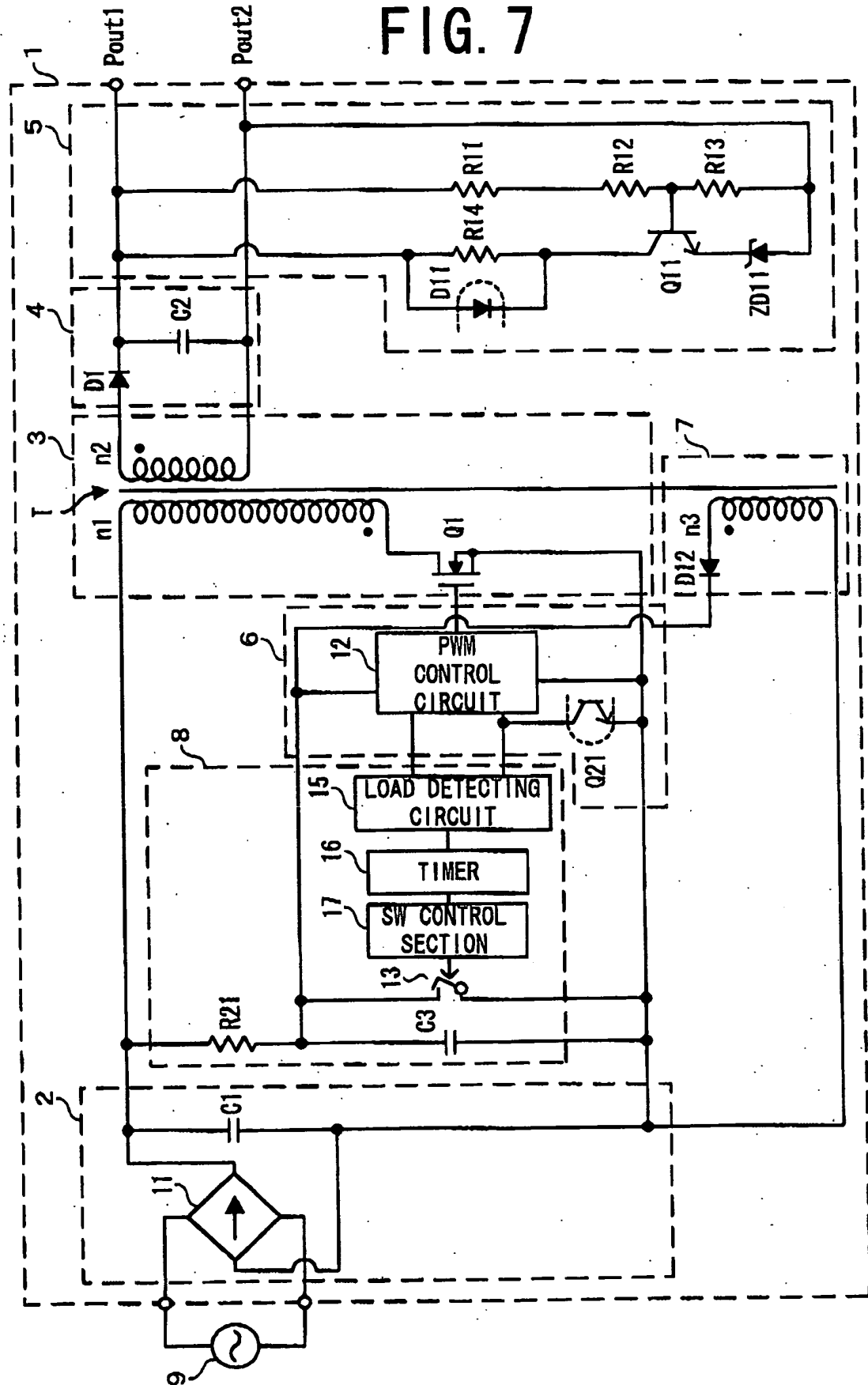
Key voltage levels and transitions are marked:  $V_1$  is the initial high level;  $V_{ref}$  is the reference voltage level; and  $V_{pc}$  is the peak-to-peak voltage level. The transitions at  $t_{21}$ ,  $t_{22}$ , and  $t_{23}$  are marked with asterisks (\*).

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FIG. 6

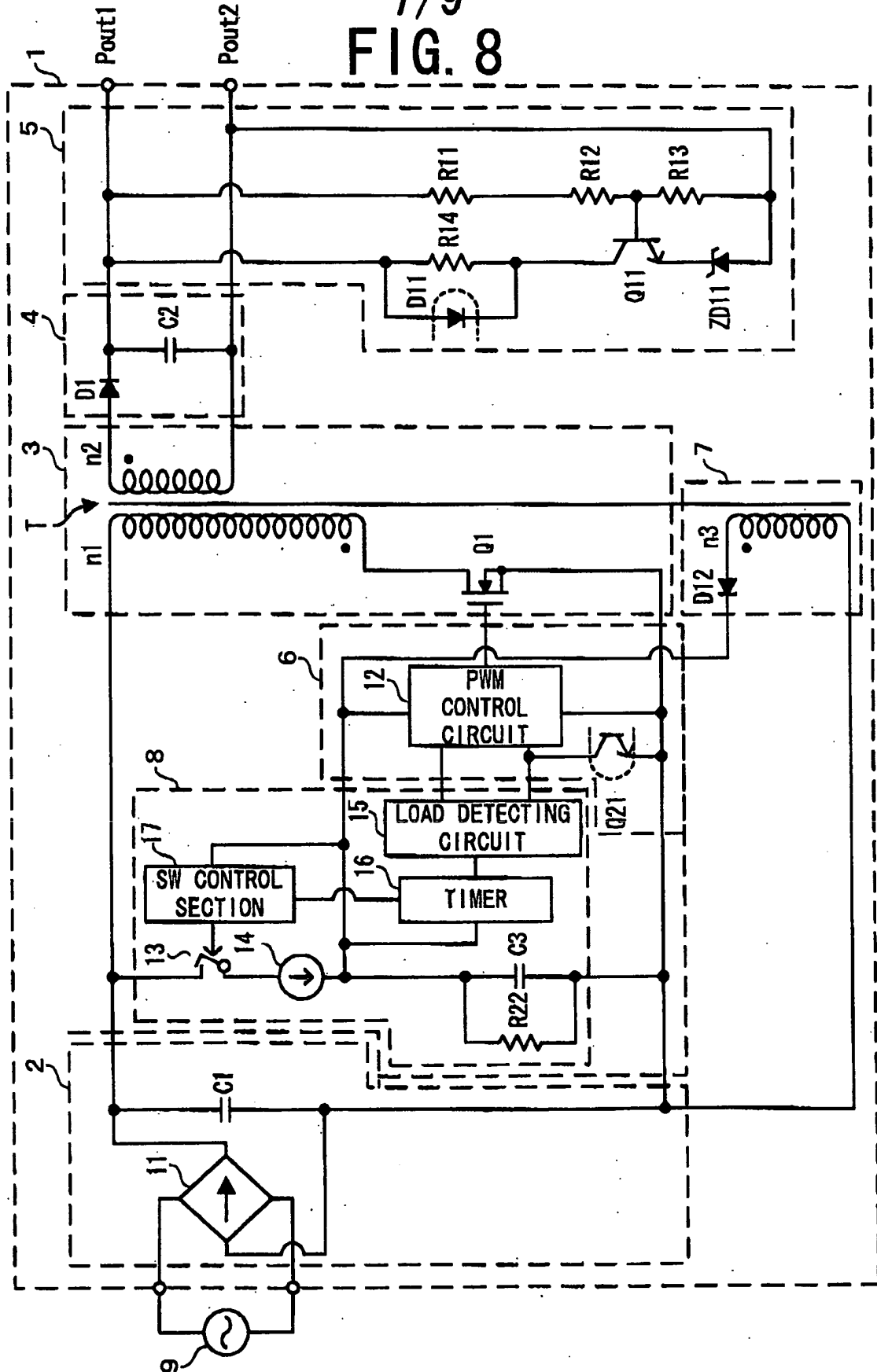


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FIG. 7



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FIG. 8



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FIG. 9

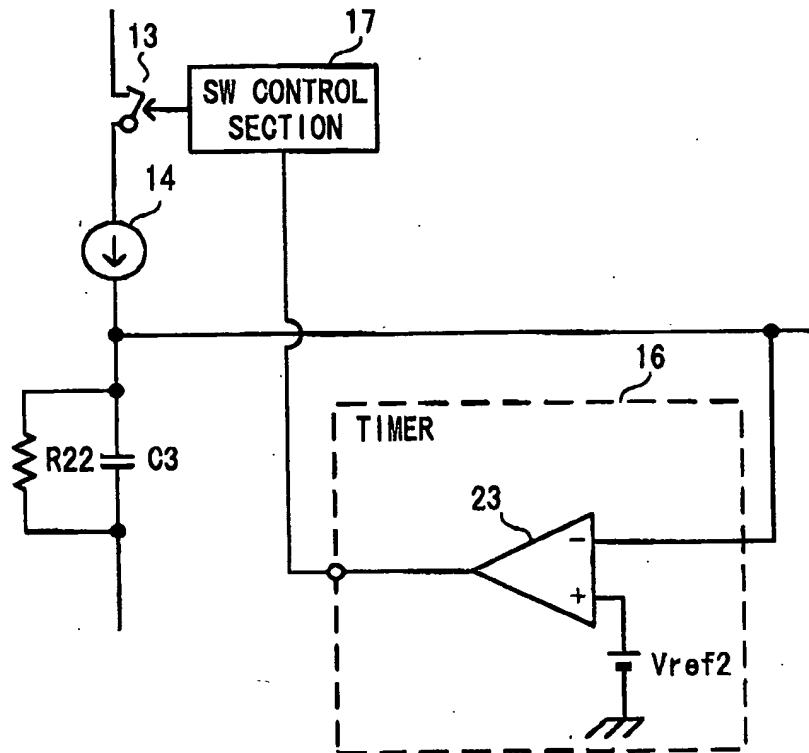
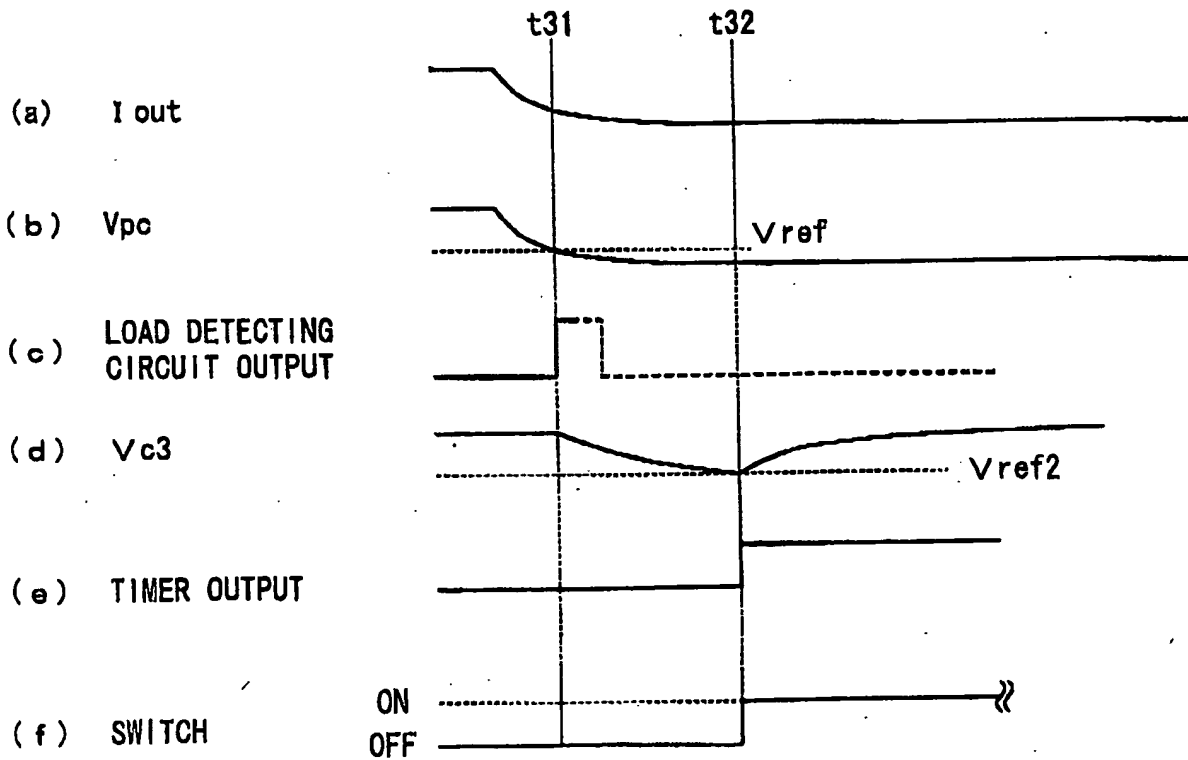


FIG. 10





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FIG. 11

